AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (currently amended): An automated integrated circuit design method comprising:

(a) defining performance specifications for a circuit formed from a plurality of interconnected circuit devices;

(b) defining at least one constraint on the relative placement of each circuit device with respect to at least one other circuit device;

(c) laying out the circuit devices subject to each constraint, wherein each circuit device is assigned an initial size that establishes an initial value of a device parameter therefor;

(d) determining initial values of performances for the circuit from the layout of the circuit devices;

(e) determining for each performance, device parameter pair, a ratio of changes of the values thereof,

(f) ~~if~~ determining that at least one performance is not within a predetermined tolerance of the corresponding performance specification[[,]] and choosing one of the circuit devices;

(g) resizing the chosen circuit device;

(h) determining an updated value of the device parameter for the resized circuit

device;

(i) determining a first value between the updated value of the device parameter and the initial value of said device parameter;

(j) for each ratio associated with the initial value of the device parameter having its value updated in step (h), combining said ratio with said first value to obtain a second value;

(k) for each ratio having the second value determined therefor in step (j), combining said second value with the initial value of the performance associated with said ratio to determine an updated value for said performance; and

(l) repeating steps (f) - (k) until the performances are within the predetermined tolerances of the performance specifications.

Claim 2 (original): The method of claim 1, wherein step (e) includes forming an array of ratios, wherein each ratio represents changes in the value of the corresponding performance as a function of changes in the value of the corresponding device parameter.

Claim 3 (original): The method of claim 1, further including, when the performances are within the predetermined tolerances of the performance specifications, outputting the layout of the circuit devices, including the size of each device, associated with the performances as the circuit design.

Claim 4 (original): The method of claim 1, wherein:

step (c) further includes routing conductors to electrically interconnect the laid out circuit devices and determining for each routed conductor an electrical parasitic effect associated therewith; and

step (d) includes determining the performances for the circuit based on the size of each device and the electrical parasitic effect of each conductor.

Claim 5 (original): The method of claim 1, wherein step (f) includes randomly choosing the one circuit device.

Claim 6 (original): A computer readable medium having stored thereon instructions which, when executed by a processor, cause the processor to:

(a) receive performance specifications for a circuit formed from a plurality of interconnected circuit devices;

(b) receive at least one constraint on the relative placement of each circuit device with respect to at least one other circuit device;

(c) layout the circuit devices subject to each constraint, wherein each circuit device is assigned a size that establishes at least one device parameter therefor;

(d) determine performances of the circuit from the layout of the circuit devices;

(e) define a relationship between each performance and each device parameter;

(f) if at least one performance is not within a predetermined tolerance of the corresponding performance specification, choose one circuit device;

(g) resize the chosen circuit device;

(h) determine a change in at least one device parameter for the resized circuit device;

(i) determine for each change in step (h) a change in at least one performance based on at least one relationship defined in step (e); and

(j) repeat steps (f) - (i) until the performances are within the predetermined tolerances of the performance specifications.

Claim 7 (original): The computer readable medium of claim 6, wherein step (e) includes forming an array of ratios of changes of performance versus changes of device parameters, wherein each

ratio represents changes in value of one performance as a function of changes in value of one device parameter.

Claim 8 (original): The computer readable medium of claim 6, wherein the instructions cause the processor to perform the further step of:

output as the circuit design the layout of the circuit devices, including the size of each device, associated with the performances when said performances are within the predetermined tolerances of the performance specifications.

Claim 9 (original): The computer readable medium of claim 6, wherein:

step (c) further includes route conductors to electrically interconnect the laid out circuit devices and determine for each routed conductor an electrical parasitic effect associated therewith; and

step (d) includes determine the performance specifications for the circuit based on the size of each device and the electrical parasitic effect of each conductor.

Claim 10 (currently amended): An automated integrated circuit design method comprising:

(a) defining performance specifications for a circuit formed from a plurality of interconnected circuit devices;

(b) defining at least one constraint on the relative placement of each circuit device with respect to at least one other circuit device;

(c) laying out the circuit devices subject to each constraint, wherein each circuit device is assigned a size that establishes at least one device parameter therefor;

(d) routing conductors to electrically interconnect the laid out circuit devices whereupon the routing of each conductor establishes an electrical parasitic effect therefor;

(e) determining performances for the circuit from the layout of the circuit devices and the routing of the conductors;

(f) defining a relationship for each performance, device parameter pair;

(g) defining a relationship for each performance, parasitic effect pair;

(h) ~~if~~ determining that at least one performance is not within a predetermined tolerance of the corresponding performance specification[[,]] and choosing one circuit device;

(i) resizing or repositioning the chosen circuit device;

(j) in response to resizing the one circuit device, repeating steps (h) and (i) after determining a change in at least one performance of the one circuit device utilizing at least one relationship defined in step (f); and

(k) in response to repositioning the one circuit device, repeating steps (h) and (i) after determining a change in at least one performance of the one circuit device utilizing at least one relationship defined in step (g).

Claim 11 (original): The method of claim 10, further including outputting as the circuit design the layout of the circuit devices associated with the performances when said performances are within predetermined tolerances of the performance specifications.

Claim 12 (original): The method of claim 10, wherein step (e) includes determining the performances of the circuit based on the size of each device and the parasitic effect of each conductor.

Claim 13 (original): The method of claim 10, wherein step (f) includes forming an array of ratios, wherein each ratio represents changes in the value of one of the performances as a function of changes in the value of one of the device parameters.

Claim 14 (original): The method of claim 10, wherein step (g) includes forming an array of ratios, wherein each ratio represents changes in the values of one of the performances as a function of changes in the value of one of the parasitic effects.

Claim 15 (new): A method for designing integrated circuits, comprising:

defining performance specifications for a circuit formed from a plurality of interconnected circuit devices;

defining at least one constraint on the relative placement of each circuit device with respect to at least one other circuit device;

laying out the circuit devices subject to each constraint, wherein each circuit device is assigned a size that establishes a device parameter therefor;

routing conductors to electrically interconnect the laid out circuit devices whereupon the routing of each conductor establishes an electrical parasitic effect therefor;

determining performances for the circuit from the layout of the circuit devices and the routing of the conductors;

determining at least one relationship for changes in at least one performance, device parameter pair or at least one performance, parasitic effect pair; and

improving at least one performance that is not within a predetermined tolerance of the corresponding performance specification by adjusting at least one circuit device or at least one

conductor and determining a corresponding performance change according to the determined at least one relationship between changes in the values thereof.

Claim 16 (new): The method of claim 15, wherein the at least one relationship includes an array of ratios that measure changes in performance values over changes in device parameter values.

Claim 17 (new): The method of claim 15, wherein the at least one relationship includes an array of ratios that measure changes in performance values over changes in electrical parasitic effect values.

Claim 18 (new): The method of claim 15, wherein improving at least one performance that is not within a predetermined tolerance of the corresponding performance specification includes resizing a chosen circuit device and updating at least one corresponding device parameter.

Claim 19 (new): The method of claim 15, wherein improving at least one performance that is not within a predetermined tolerance of the corresponding performance specification includes repositioning a chosen device and updating at least one corresponding conductor routing.

Claim 20 (new): A computer-readable medium that stores a computer program for designing integrated circuits, wherein the computer program includes instructions for:

defining performance specifications for a circuit formed from a plurality of interconnected circuit devices;

defining at least one constraint on the relative placement of each circuit device with respect to at least one other circuit device;

laying out the circuit devices subject to each constraint, wherein each circuit device is assigned a size that establishes a device parameter therefor;

routing conductors to electrically interconnect the laid out circuit devices whereupon the routing of each conductor establishes an electrical parasitic effect therefor;

determining performances for the circuit from the layout of the circuit devices and the routing of the conductors;

determining at least one relationship for changes in at least one performance, device parameter pair or at least one performance, parasitic effect pair; and

improving at least one performance that is not within a predetermined tolerance of the corresponding performance specification by adjusting at least one circuit device or at least one conductor and determining a corresponding performance change according to the determined at least one relationship between changes in the values thereof.

Claim 21 (new): The computer-readable medium of claim 20, wherein the at least one relationship includes an array of ratios that measure changes in performance values over changes in device parameter values.

Claim 22 (new): The computer-readable medium of claim 20, wherein the at least one relationship includes an array of ratios that measure changes in performance values over changes in electrical parasitic effect values.

Claim 23 (new): The computer-readable medium of claim 20, wherein improving at least one performance that is not within a predetermined tolerance of the corresponding performance specification includes resizing a chosen circuit device and updating at least one corresponding device parameter.

Claim 24 (new): The computer-readable medium of claim 20, wherein improving at least one performance that is not within a predetermined tolerance of the corresponding performance specification includes repositioning a chosen device and updating at least one corresponding conductor routing.